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1	BRS	L1	5	memory with ((back adj gate) near5 (potential or bias or volt\$3)) with writ\$3 with read\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
2	BRS	L2	1	memory with substrate with (potential or bias or volt\$3) with chang\$3 with (back adj gate) with response with mode with operat\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
3	BRS	L3	1	memory with substrate with (potential or bias or volt\$3) with chang\$3 with (back adj gate) and (response with mode with operat\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
4	BRS	L4	83	memory with substrate with (potential or bias or volt\$3) and chang\$3 and (back adj gate) and (response with mode with operat\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB
5	BRS	L5	12	memory with substrate with (potential or bias or volt\$3) and (chang\$3 with (back adj gate)) and (response with mode with operat\$3)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB

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DBs US-PGPUB: USPAT: USOCR: EPO: JPO: DERWENT: IBM_TDB

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